LOW-VOLTAGE JOYSTICK PORT INTERFACE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a low-voltage joystick port interface and a method of interfacing a standard-voltage joystick with a low-voltage port of a processor.

2. Description of Prior Art

As a peripheral device, a user manipulated joystick enables the real-time interaction between a user and a host computer which is necessary for certain computer applications (e.g., computer games). The joystick typically includes a potentiometer for each orthogonal coordinate axis. The resistance of the potentiometer varies in direct relation to the joystick handle position along the corresponding coordinate axis. Each potentiometer has a first terminal connected to a 5 Volt supply. To provide digital values which may be processed by the host computer, a second terminal of the joystick potentiometer is connected to a joystick port interface.

As illustrated in Fig. 1, the prior art joystick port interface 120 (illustrated for a single coordinate axis only, e.g., the X-axis) includes a quad timer 126 and a "recommended" Resistor-Capacitor (RC) network having a resistor 122 (typically R = 2.26 kilohms) and a capacitor 124 (typically C = 10nF). A first terminal of the RC network resistor 122 is serially coupled to the joystick potentiometer 112, while the other

terminal of the RC network resistor 122 is coupled to a node A. A first terminal of the RC network capacitor 124 is coupled to the node A, while the other terminal of the RC network capacitor 124 is connected to ground. The quad timer 126 is coupled to the node A, and receives the analog voltage level, JSout, across the RC network capacitor 124. The quad timer 126 includes an analog comparator (not shown) which compares JSout with a predetermined threshold voltage Vt (typically 3.34 Volts) and outputs a pulse signal P_i to the host computer.

Upon receiving a request from the host computer, the quad timer 126 discharges the RC network capacitor 124 and sets P_i to a logic "1" level. As current passes though the joystick potentiometer 112, the RC network capacitor 124 charges until Vt is reached. At this time the quad timer 126 sets P_i back to a logic "0" level. The pulse width of P_i thus represents the time interval, T, required to charge the RC network capacitor 124 to the threshold voltage Vt. The pulse width of P_i is monitored by the host computer to indicate the resistance of the joystick potentiometer 112 which, as discussed above, has a direct relation to the coordinate position of the joystick 110.

For the conventional joystick port interface described above, both the joystick 110 and the quad timer 126 utilize a 5 Volt power supply. The power supply for the next generation of integrated circuits, however, will be substantially less than 5 Volts, and therefore a low-power port is needed to interface the conventional 5 Volt joystick device with a lower-Volt integrated circuit such as a CMOS (complementary metal-oxide silicon) VLSI (very large-scale integration) circuit.

SUMMARY OF THE INVENTION

The joystick port interface according the present invention is a low power port which interfaces a typical 5 Volt joystick peripheral device with a lower power computer port. The low-voltage joystick port interface includes a bidirectional buffer circuit and a pulse generator which, together, generate a digital pulse signal, representing a joystick coordinate position, based on an input analog measurement signal.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings which are given by way of illustration only, wherein like reference numerals designate corresponding parts in the various drawings, and wherein:

Fig. 1 illustrates a prior art joystick port interface;

Fig. 2 illustrates the joystick port interface according to the present invention; and

Fig. 3 illustrates the relationship between various signal levels of the joystick port interface illustrated in Fig. 2.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The following detailed description relates to a joystick port interface and a method of interfacing a standard-Volt (e.g., 5 Volt) joystick with a low-power processor (e.g., less than 5 Volt) port. For the purposes of discussion only, the processor will be described as being a host computer. Fig. 2 illustrates a joystick port interface according to the present invention. As shown in Fig. 2, the joystick port interface includes the RC network components discussed above with reference to Fig. 1, namely the RC network

resistor 122 and the RC network capacitor 124. The joystick interface according to the present invention further includes a low-voltage interface circuit 200 which includes two main components: a latch 202 and a bidirectional buffer circuit 220. The bidirectional buffer circuit 220 includes a three-state buffer 222 and an input buffer 224. The interface circuit 200 further includes a bidirectional input/output (I/O) terminal 206 and certain logic elements, namely an inverter 204 and an AND gate 208.

The latch 202 is a D-type flip-flop having a total of four inputs: preset PRN, data D (fixed at a logic "1" level), clock CK, and clear CDN. The latch 202 has two outputs, Q and QB (the complement of Q). As will be described in detail below, the latch 202 functions as a pulse generator so that the output QB signal, which the host computer receives as a pulse signal PCin, represents the time interval, T, needed to charge the RC network capacitor 124 to a threshold voltage level, Vtnew, of the input buffer 224.

The interface circuit 200 receives a pair of control signals from the host computer, namely a RESET signal and a WRITTEN signal. The latch 202 receives the WRITTEN signal from the host computer at the clear CDN input, and receives the RESET signal from the host computer at the preset PRN input via the inverter 204. In other words, an input node of the inverter 204 directly receives the RESET signal from the host computer, and the inverter 204 outputs an inverted RESET signal to the preset PRN input of the latch 202. The clock CK input of the latch 202 receives the output of the input buffer 224.

A first input node of the AND gate 208 receives the inverted RESET signal output by the inverter 204. A second input node of the AND gate 208 receives the output Q signal from the latch 202. A control node C of the three-state buffer 222 receives the output of

the AND gate 208, and a data input node of the three-state buffer 222 is set to a logic "0" level. The output of the three-state buffer 222 is coupled to a node B, which also connects to one end of the bidirectional I/O terminal 206. The bidirectional I/O terminal 206 is connected to the node A of the external RC network described above with reference to Fig. 1 so that JSout is received by the interface circuit 200.

The three-state buffer 222 operates in either a high impedance state (when the AND gate 208 outputs a logic "0" level signal) or an active state (when the AND gate 208 outputs a logic "1" level signal). In the high impedance state, the three-state buffer 222 essentially operates as an open circuit, thus allowing the RC network capacitor 124 to charge as current passes through the joystick potentiometer. On the other hand, when the three-state buffer 222 is active, it will always drive the I/O terminal 206 to ground, thus essentially acting as a pull-down device which causes the RC network capacitor 124 to discharge. In other words, the three-state buffer 222 has sufficient current sinking capability to overdrive the elements outside the interface circuit 200, and drive the I/O terminal 206 to ground.

The input buffer 224 has a threshold voltage level Vtnew (e.g., 3.3 Volts). When JSout is less than Vtnew, the input buffer 224 outputs a logic "0" level signal. On the other hand, when JSout exceeds Vtnew, the input buffer 224 outputs a logic "1" level signal. Since JSout has a long time constant which can be susceptible to noise, the input buffer 224 has a hysteresis level that is greater than the expected noise level, thereby preventing short duration pulses from disrupting the joystick port operation.

The operation of the joystick port interface illustrated in Fig. 2 will be described as follows. The joystick port interface operates in a plurality of

states which will be discussed in turn.

When idle, the joystick port interface is said to operate in a disabled state. During this disabled state, the host computer outputs a logic "1" level RESET signal to the inverter 204, and thus the three-state buffer 222 enters the high impedance state. More specifically, the first input node of the AND gate 208 receives a logic "0" level signal via the inverter 204. Consequently, the AND gate 208 outputs a logic "0" control signal to the three-state buffer 222. As discussed above, when the control node C of the three-state buffer 222 receives a logic "0" level signal via the AND gate 208, the three-state buffer 222 enters a high-impedance state. During this state, JSout gradually rises as the RC network capacitor 124 charges, eventually reaching a maximum level of 5 Volts.

Because the host computer outputs a logic "1" level RESET signal during the disabled state, the preclear PRN input to the latch 202 receives a logic "0" level signal via the inverter 204, resulting in a logic "1" level output Q signal, regardless of the other inputs to the latch 202. Consequently, the pulse signal PCin received by the host computer is set to a logic "0" level, even when JSout exceeds the threshold voltage Vtnew of the input buffer 224.

To enter a standby state, in which the joystick port interface is prepared to provide a joystick position pulse to the host computer, the host computer switches the RESET signal from a logic "1" level to a logic "0" level, and thus the first and second input nodes of the AND gate 208 respectively receive a logic "1" level signal from the inverter 204 and a logic "1" level signal from the output Q of the latch 202. Consequently, the AND gate 208 outputs a logic "1" level signal to the control node C of the three-state buffer 222. As described above, the three-state buffer

222 enters an active state when the control node C receives a logic "1" level signal from the AND gate 208, thereby driving the I/O terminal 206 to ground and causing the RC network capacitor 124 to discharge. As the RC network capacitor 124 discharges, JSout drops below the threshold voltage Vtnew of the input buffer 224 and the clock CK input of the latch 202 switches to a logic "0" level, thereby closing the latch 202. The output Q signal remains at a logic "1" level, and consequently the PCin signal remains at a logic "0" level as illustrated in Fig. 3.

After a sufficient time has passed for the RC network capacitor 124 to fully discharge, the joystick port interface has reached the standby state. When the host computer subsequently requests a joystick position pulse, the joystick port interface is said to operate in a pulse-generating state. To initiate this pulse-generating state, the host computer switches the WRITTEN signal from a logic "1" level to a logic "0" level, and then back to a logic "1" level as illustrated in Fig. 3. When the WRITTEN signal is at a logic "0" level, the clear CDN input to the latch 202 is at a logic "0" level so that the output Q signal of the latch 202 switches to a logic "0" level, regardless of the remaining inputs to the latch 202 (i.e., the latch 202 clears) and the pulse signal PCin is at a logic "1" level as illustrated in Fig. 3. Since the output Q signal is at a logic "0" level, the AND gate 208 again outputs a logic "0" level signal to the three-state buffer 222, thereby rendering the three-state buffer 222 inactive and allowing the RC network capacitor 124 to charge.

When JSout reaches Vtnew, the input buffer 224 outputs a logic "1" level signal to the clock CK input of the latch 202, thus opening the latch 202. In other words, the output Q signal of the latch 202 switches from a logic "0" level to a logic "1" level, and

consequently the pulse signal PCin switches back from a logic "1" level to a logic "0" level as illustrated in Fig. 3. The duration that PCin remains at a logic "1" level indicates the joystick potentiometer resistance for the corresponding coordinate axis.

The output of the AND gate 208 again switches from a logic "0" level to a logic "1" level, causing the three-state buffer 222 to switch from the high impedance state to the active state. Consequently, the three-state buffer 222 again drives the I/O terminal 206 to ground, causing the RC network capacitor 124 to discharge. Therefore, the joystick port interface automatically returns to the standby state and is ready for subsequent attempts to sense the joystick coordinate positions. The operation described above automatically reconfigures the joystick port interface to the standby state in which the output Q signal of the latch 202 is a logic "1" level and the RC network capacitor 124 discharges. Consequently, the joystick port interface does not "lockup" in an unusable state.

The joystick port interface described above can be implemented using all standard CMOS VLSI structures, without requiring special design tolerances. Furthermore, this implementation results in zero power dissipation when disabled and prevents the joystick port interface from entering into an unrecoverable state.

As a final matter, although Vtnew has been shown by way of example as being 3.3 Volts, other values for Vtnew are acceptable. For example, Vtnew may be substantially less than 3.3. Volts (e.g., 2.5 Volts). Naturally, the time required for Jsout to reach the input buffer threshold level ("rise time") will vary in direct relation to Vtnew. The pulse width of the PCin signal, which represents rise time, however, should not be less than or exceed expected minimum/maximum pulse width values. Therefore, to ensure optimal joystick

position sensing, the capacitance ("Cnew") of the RC network capacitor 124 may be selected in relation to Vtnew.

In other words, Cnew is set so that the pulse width of PCin conforms to expected minimum/maximum values. Specifically, Cnew is selected according to the following formula:

$$Cnew = \frac{11nF}{\ln\left(\frac{5V}{5V - Vtnew}\right)} \quad for\ Vtnew < 5.0\ Volts. \qquad (1)$$

As mentioned above, Cnew represents the new capacitance of the RC network capacitor 124 and Vtnew represents the threshold level of the input buffer 224.

The invention being thus described, it will be obvious to one skilled in the art that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications are intended to be included within the scope of the following claims.